REMARKS

Applicants respectfully request reconsideration of this application in view of the foregoing amendment and following remarks.

Status of the Claims

Claims 1-17 are pending in this application. Claims 1 and 2 are independent. All of the pending claims stand rejected. By this amendment, claims 1 and 2 are amended. New claim 18 is added. No new matter has been added by this amendment.

Rejection under 35 U.S.C. §102

In paragraph three (3) of the Office Action, claims 1-6, 10-13 and 17 have been rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,972,635 to McCorquodale et al. ("McCorquodale").

McCorquodale discloses a MEMs-based clock generation circuit (i.e., an oscillator) including a high-Q MEMS LC-tank apparatus for generating a periodic signal, a first circuitry for converting the periodic signal into a high frequency digital output signal and a second circuitry for dividing the frequency of the digital output signal to at least one lower desired application frequency. McCorquodale teaches that the LC-tank apparatus, first circuitry and second circuitry are formed on a same substrate (e.g., col. 13, lines 23-40). The Examiner indicates, *inter alia*, that McCorquodale discloses in Figs. 7c and 8a, along with relevant portions of the specification, each and every element of claims 1-6, 10-13 and 17.

Independent claims 1 and 2 have been amended for further clarification. In particular, amended claim 1 recites, *inter alia*, "a PLL synthesizer having a phase detector and a control voltage generation circuit, wherein the phase detector is configured to detect phase difference

between the output signal from the voltage controlled oscillator and a reference signal, and the control voltage generator circuit is configured to generate a control signal of the voltage controlled oscillator based on the phase information detected at the phase detector so that the voltage controlled oscillator is controlled to generate the output signal having a frequency of n times of a target frequency." Amended claim 1 further recites "a frequency divider circuit dividing the output signal from the voltage controlled oscillator into 1/n frequency."

Amended claim 2 recites similar features to amended claim 1 as discussed herein, e.g., a voltage controlled oscillator that generates an output signal having a frequency of n times of a target frequency, a PLL synthesizer, and a separate frequency divider that divides the output signal from the oscillator into 1/n frequency.

Referring to Figs 1 and 2 and relevant portions of the original specification (e.g., the first full paragraph of page 12 (lines 4-17)), an oscillating unit 11 and a PLL synthesizer 21 are coupled in such a way that an output from the oscillating unit is inputted to the PLL synthesizer and the PLL synthesizer generates a control voltage signal (i.e., Vt) to be inputted to the oscillating unit. In response, the oscillating unit generates an output signal having a frequency of n times of a target frequency. The output signal from the oscillating unit is then inputted to the divider 22 to convert the frequency into the target frequency (i.e., 1/n frequency). One of the aspects of the present invention is directed to an oscillator circuit designed to generate a signal having a frequency n times higher than a target frequency so that the required values of the inductance and capacitance are formed on an IC board. See the first full paragraph of page 11 (i.e., lines 11-18) of the original specification. The n times higher frequency signal generated

from the oscillator circuit is then divided into a target frequency (i.e., 1/n frequency) at a frequency divider located outside the PLL.

As Applicants understand it, McCorquodale fails to show or suggest an oscillating circuit having a separate PLL synthesizer configured to provide a control signal to the oscillator as discussed above.

Accordingly, each of amended claims 1 and 2, and claims dependent therefrom (i.e., claims 3-6, 10-13 and 17) is believed neither anticipated by nor rendered obvious in view of the cited art of record (i.e., McCorquodale) for at least the reasons discussed above.

Reconsideration and withdrawal of the rejections of claims 1-6, 10-13 and 17 under 35 U.S.C. §102(e) is respectfully requested.

Rejection under 35 U.S.C. §103

In paragraph six (6) of the Office Action, claims 7-9 and 14-16 have been rejected under 35 U.S.C. §103(a) as being unpatentable over McCorquodale in view of U.S. Patent No. 6,362,698 to Gupta ("Gupta") and U.S. Patent No. 6,268,778 to Mucke et al. ("Mucke").

Gupta is cited as disclosing a prior art PLL system and Mucke is cited as disclosing the use of integrated type capacitance elements formed by MOSFETs. However, none of the additionally cited references show or suggest a PLL system and a separate frequency divider configured in such a way as recited in amended claims 1 and 2 as discussed above from which the rejected claims depend.

Accordingly, each of claims 7-9 and 14-16 is believed neither anticipated by nor rendered obvious in view of the cited art of record (i.e., McCorquodale, Gupta and Mucke), either taken alone or in combination, for at least the reasons discussed above for claim 1.

Reconsideration and withdrawal of the rejections of claims 7-9 and 14-16 under 35 U.S.C. §103(a) is respectfully requested.

New Claim

New claim 18 has been added to recite the claimed invention in an alternative way. Since new claim 18 depends from claim 1 as amended, it is also believed to be allowable over the cited art of record for at least the similar reasons as discussed above for claim 1.

Applicants believe that the application is in condition for allowance and such action is respectfully requested.

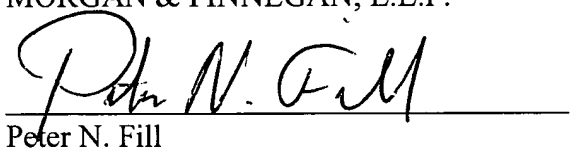
AUTHORIZATION

No petitions or additional fees are believed due for this amendment and/or any accompanying submissions since the shortened statutory due date falls on Saturday (i.e., June 24, 2006). However, to the extent that any additional fees and/or petition is required, including a petition for extension of time, Applicants hereby petition the Commissioner to grant such petition, and hereby authorizes the Commissioner to charge any additional fees, including any fees which may be required for such petition, or credit any overpayment to Deposit Account No. 13-4500 (Order No. 5000-5247). A DUPLICATE COPY OF THIS SHEET IS ENCLOSED.

An early and favorable examination on the merits is respectfully requested.

Respectfully submitted,
MORGAN & FINNEGAN, L.L.P.

Dated: June 26, 2006

By: 

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